

REMARKS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-31 are presently active in this case. The present Amendment amends Claim 1 without introducing any new matter.

The outstanding Office Action objected to Claim 1 because of informalities. Claims 1 and 16 were rejected under 35 U.S.C. §103(a) as unpatentable over Nikutta et al. (U.S. Patent No. 5,821,804, herein "Nikutta") in view of Liu et al. (U.S. Patent No. 6,947,267, herein "Liu"). Claims 2-15 and 17-31 were indicated as allowable if rewritten in independent form.

Applicant acknowledges with appreciation the indication of allowable subject matter. However, since Applicant considers that Claims 1 and 16, from which Claims 2-15 and 17-31 depend, defines patentable subject matter, Claims 1 and 16 are maintained in dependent form at the present time.

Initially, Applicant respectfully requests that the references cited in the Information Disclosure Statement (IDS) filed September 29, 2003 and February 17, 2004 be acknowledged as having been considered in the next Office Action. The references AO and AP of the February 17, 2004 IDS correspond to the U.S. Patents 5,821,804 and 5,079,612, respectively, and Applicant has also provided a Statement of Relevancy for these references. Further, the references AO, AP and AQ of the IDS filed on September 29, 2003 were also submitted with a Statement of Relevancy explaining the materiality of the respective references, to comply with the requirements under 37 C.F.R. §1.56(a). Therefore, Applicant believes that no translation for these references is required.

In response to the objection to Claim 1, Claim 1 is amended to correct the noted informalities, to recite "connects in common an output node" instead of "connects to each other output nodes," as proposed by the outstanding Office Action. Since this change is

merely formal in nature, it is not believed to raise a question of new matter. If, however, the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work with the Examiner in a joint effort to derive mutually acceptable language.

In response to the rejection of Claims 1 and 16 under 35 U.S.C. §103(a), Applicant respectfully requests reconsideration of this rejection and traverses the rejection, as discussed next.

Briefly recapitulating, Applicant's Claim 1 relates to an electrostatic discharge protection circuit device. The device includes, *inter alia*: a first electrostatic discharge protection circuit connected between a first external terminal and a first ground terminal; a second electrostatic discharge protection circuit connected between a second external terminal and a second ground terminal; a ***trigger signal line which connects in common an output node of surge detection circuits*** of the first and second electrostatic discharge protection circuits, and transfers a surge detection output of one of the first and second electrostatic discharge protection circuits to the other electrostatic discharge protection circuit as a trigger signal; and a common discharge line connected directly to the first ground terminal, connected to the second ground terminal via a parallel circuit composed of a forward-connected parasitic diode element and a reverse-connected parasitic diode element, and used commonly by the first and second of electrostatic discharge protection circuits.

As explained in Applicant's specification at page 25, line 16 to page 27, line 10 with corresponding Figure 1, Applicant's invention improves upon background electrostatic discharge protection circuit devices, since a trigger signal line connects an output node of surge detection circuits of the first and second electrostatic discharge protection circuits together, a surge detection output of one of the first and second electrostatic discharge protection circuits to the other electrostatic discharge protection circuit as a trigger signal. As a result, not only an internal circuit corresponding to one electrostatic discharge protection

circuit is protected, but also an internal circuit corresponding to the other electrostatic discharge protection circuit is protected against a surge input.

Turning now to the applied references, Nikutta discloses an integrated semiconductor formed on a substrate, wherein protective circuits are formed on the substrate and are each assigned to one of the circuit portions for preventing overvoltage.¹ Nikutta however fails to teach or suggest Applicant's claimed electrostatic discharge protection circuit devices. In particular, and as acknowledged by the outstanding Office Action,² Nikutta fails to teach or suggest a *trigger signal line which connects in common an output node* of surge detection circuits of the first and second electrostatic discharge protection circuits, and transfers a surge detection output of one of the first and second electrostatic discharge protection circuits to the other electrostatic discharge protection circuit as a trigger signal, as recited in Applicant's Claim 1.

The outstanding Office Action rejects Applicant's Claim 1 based on the proposition that Liu discloses the above feature,³ and that it would have been obvious to modify Nikutta by importing this feature from Liu to arrive at Applicant's claimed invention. Applicant respectfully submits, however, that Liu fails to disclose the above feature related to the trigger signal line, as next discussed.

The outstanding Office Action relies on Liu's text at column 5, lines 51-58 and on Figure 4. This passage of Liu describes a first and second NMOS transistor arranged in parallel, both separately coupled to a first and second low voltage source Vss1 and Vss2 and fed by two different power supplies Vcc1 and Vcc2.⁴ Reading Liu in this passage and by looking at Liu's Figure 7, a person of ordinary skill in the art would understand that a trigger signal line to one transistor N1 is isolated from the trigger signal line connected to the other

¹ See Nikutta in the Abstract and in Figure 1.

² See outstanding Office Action at page 3, lines 4-10.

³ See outstanding Office Action at page 3, lines 11-17.

⁴ See Liu at column 5, lines 53-57 and in Figures 4 and 7.

transistor N2. Accordingly, two separate trigger lines from transistors of two ESD protection devices, as taught by Liu, *is not* a trigger signal line which connects in common an output node of surge detection circuits of the first and second electrostatic discharge protection circuits, as recited in Applicant's Claim 1.

Therefore, even if the combination of Nikutta and Liu is assumed to be proper, the combination fails to teach every element of the claimed invention. Specifically, the combination fails to teach the claimed trigger signal line which connects in common an output node of surge detection circuits. Accordingly, Applicant respectfully traverses, and requests reconsideration of, this rejection based on these patents.⁵

Independent Claim 16 recites limitations analogous to the limitations recited in independent Claim 1. Accordingly, for the reasons stated above for the patentability of Claim 1, Applicant respectfully submits that the rejections of Claim 16, and all associated dependent claims, are also believed to be overcome in view of the arguments regarding independent Claim 1.

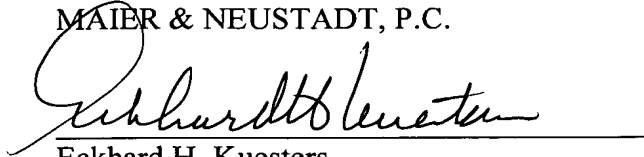
Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal Allowance. A Notice of Allowance for Claims 1-31 is earnestly solicited.

⁵ See MPEP 2142 stating, as one of the three "basic criteria [that] must be met" in order to establish a *prima facie* case of obviousness, that "the prior art reference (or references when combined) must teach or suggest all the claim limitations," (emphasis added). See also MPEP 2143.03: "All words in a claim must be considered in judging the patentability of that claim against the prior art."

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, the Examiner is encouraged to contact Applicant's undersigned representative at the below listed telephone number.

Respectfully submitted,

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